WHAT IS CLAIMED IS:

1. A method of distributing packets among a plurality of processing devices, the method comprising:

receiving a packet;

inputting at least a portion of the packet into a content addressable memory; and

obtaining a result from the content addressable memory to indicate a selected processing device to which the received packet is to be sent; and

sending the received packet to the indicated processing device.

2. A method as recited in claim 1, wherein the selected device is selected from a plurality of cache systems.

3. A method as recited in claim 1, wherein the result indicates to redirect the packet from being sent to a destination specified in the received packet.

4. A method as recited in claim 3, wherein the result includes a processing device identification corresponding to the selected device to which the received packet is to be sent.

5. A method as recited in claim 1, wherein the content addressable memory is a ternary content addressable memory.

6. A method as recited in claim 1, wherein the portion(s) of the received packet input into the content addressable memory is selected from a group consisting of a destination address, a destination port, a source address, a source port, and a protocol.

7. A method as recited in claim 1, wherein the TCAM includes a plurality of entries, and each entry includes a bits-to-match field, an action field, and a redirection destination field.

8. A method as recited in claim 7, wherein the redirection destination field identifies a cache system.

9. A method as recited in claim 8, wherein the action field indicates whether the received packet is to be redirected.

10. A method for facilitating traffic distribution among a plurality of devices, the method comprising generating a plurality of entries within a content addressable memory, each entry including a set of bit values that correspond to at least a portion of a packet and

each entry including one or more destination fields indicating where to send a packet that matches the entry's set of bit values.

11. A method as recited in claim 10, wherein the destination fields include an action field indicating whether to redirect the packet from a destination indicated by the packet itself.

12. A method as recited in claim 11, wherein the destination fields include a destination identifier indicating a device to which the packet is to be redirected.

13. A method as recited in claim 10, wherein the set of bits values include at least a 1 or a 0 value and a "don't care" value.

14. A method as recited in claim 10, wherein the content addressable memory is ternary.

15. A computer system operable to distribute packets among a plurality of processing devices, comprising:

a first memory;

a content addressable memory; and

a processor coupled to the first memory and the content addressable memory,

wherein at least one of the first memory and the processor are adapted to provide:

receiving a packet;

inputting at least a portion of the packet into the content addressable memory; and

obtaining a result from the content addressable memory to indicate a selected processing device to which the received packet is to be sent; and

sending the received packet to the indicated processing device.

16. A computer system as recited in claim 15, wherein the selected device is selected from a plurality of cache systems.

17. A computer system as recited in claim 15, wherein the result indicates to redirect the packet from being sent to a destination specified in the received packet.

18. A computer system as recited in claim 17, wherein the result includes a processing device identification corresponding to the selected device to which the received packet is to be sent.

19. A computer system as recited in claim 15, wherein the content addressable memory is a ternary content addressable memory.

20. A computer system as recited in claim 15, wherein the at least a portion of the received packet is selected from a group consisting of a destination address, a destination port, a source address, a source port, and a protocol.

21. A computer system as recited in claim 15, wherein the content addressable memory includes a plurality of entries, and each entry includes a bits-to-match field, an action field, and a redirection destination field.

22. A computer system as recited in claim 21, wherein the redirection destination field identifies a cache system.

23. A computer system as recited in claim 22, wherein the action field indicates whether the received packet is to be redirected.

24. A computer system operable to facilitate traffic distribution among a plurality of devices, comprising:

a first memory;

a content addressable memory; and

a processor coupled to the first memory and the content addressable memory,

wherein at least one of the first memory and the processor are adapted to provide generating a plurality of entries within the content addressable memory, each entry including a set of bit values that correspond to at least a portion of a packet and each entry including one or more destination fields indicating where to send a packet that matches the entry's set of bit values.

25. A computer system as recited in claim 24, wherein the destination fields include an action field indicating whether to redirect the packet from a destination indicated by the packet itself.

26. A computer system as recited in claim 25, wherein the destination fields include a destination identifier indicating a device to which the packet is to be redirected.

27. A computer system as recited in claim 24, wherein the set of bits values include at least a 1 or a 0 value and a "don't care" value.

28. A computer system as recited in claim 24, wherein the content addressable memory is ternary.

29. A computer program product for distributing traffic, the computer program product comprising:

at least one computer readable medium;

computer program instructions stored within the at least one computer readable product configured to cause a processing device to:

receive a packet;

input at least a portion of the packet into a content addressable memory; and

obtain a result from the content addressable memory to indicate a selected processing device to which the received packet is to be sent; and

send the received packet to the indicated processing device.

30. A computer program product for distributing traffic, the computer program product comprising:

at least one computer readable medium;

computer program instructions stored within the at least one computer readable product configured to cause a processing device to generate a plurality of entries within a content addressable memory, each entry including a set of bit values that correspond to at least a portion of a packet and each entry including one or more destination fields indicating where to send a packet that matches the entry's set of bit values.

31. An apparatus for distributing traffic comprising:

a means for receiving a packet;

a means for inputting at least a portion of the packet into a content addressable memory; and

a means for obtaining a result from the content addressable memory to indicate a selected processing device to which the received packet is to be sent; and

a means for sending the received packet to the indicated processing device.

32. An apparatus for distributing traffic comprising a means for generating a plurality of entries within a content addressable memory, each entry including a set of bit values that correspond to at least a portion of a packet and each entry including one or more destination fields indicating where to send a packet that matches the entry's set of bit values.